REMARKS

The current Office Action has been reviewed and carefully considered. Claim 18 has been canceled and claims 19 and 20 have been added. Claims 1-17 and 19-20 are pending in this application, of which claims 1 and 7 are independent claims. Reconsideration of the above-identified application, as amended and in view of the following remarks, is respectfully requested.

Claim 15 rejected as indefinite. To comply with the Examiner's rejection, claim 15 has been amended. Claim 18 stands rejected under 35 U.S.C. 112, second paragraph, as indefinite. To move prosecution forward, claim 18 has been canceled without prejudice. Accordingly, the rejection of claim 18 is moot.

Claims 1-3, 5-9 and 11-13 and 15-16 stand rejected under 35 USC 103(a) as allegedly unpatentable over PCT Publication No. WO 95/10083 to Assar et al. ("Assar").

Advantageously, the present invention allows the reclaiming of free space to occur independently of events executed to efficiently regulate uniform block wear levels. When data requiring less update is shifted to a block of high wear level, subsequent update of the data at the new location is not inhibited (page 7, lines 25-29: "To avoid the block 22 being erased many times more"). The present invention recognizes that, over time, as the limit value is raised successively, any difference in wear levels will smooth out. Consequently, it is not necessary to reclaim free space every time there is an increase in the limit value against which wear counts are compared. To the contrary, free space can be reclaimed at the appropriate optimum time.

Assar, by contrast, inhibits further update of the shifted data at the new location. At the moment at which all blocks exceed the limit value, there is no alternative but to immediately reclaim free space, regardless of the system impact with regard to, for example, power requirements (Assar, page 3, lines 1-3; page 8, line 36 to page 9, line 8).

Claim 1 recites "wherein the blocks from said variety have an associated counter for counting the number of mutations in the block concerned, and a limit value is increased when a predetermined number, which is at least the majority, of the counters of the blocks from said variety exceed the limit value, said determining being based on said limit value and a value of the counter of the first block (22)."

Item 9 of the Office Action concedes that the reference does not disclose the above-shown, underlined limitation of claim 1, but alleges that increasing the limit value in lieu of clearing the counters would have been "an obvious matter of design choice." However, Assar clears the erase inhibit flags concurrently with clearing the counters. What would have been the motivation for increasing the field size for the wearout leveling count and for the limit value? Not only is more storage required, but more resources are consumed in comparing the two quantities due to their larger size. Redesigning Assar to resemble the invention as recited in claim 1 would not have been obvious for at least the above-stated reasons.

Claim 7 recites the same above-quoted limitation, and is likewise deemed to be non-obvious over Assar.

As to the art rejection of claim 15, the Office Action is rather silent and prefers to merely mention claim 15 in the same single, sentence that mentions claims 1, 7

and 13. As mentioned above, however, the specific language of claim 15 cannot properly be characterized as lacking patentable weight.

The rejection of claims 1-3, 5-9 and 11-13 and 15-16 based on Assar cannot be maintained. Reconsideration and withdrawal of the rejection is respectfully requested.

Claim 1-3, 5-9 and 11-13, 15 and 16 stand rejected under 35 U.S.C. 103(a) as unpatentable over Assar in view of U.S. Patent No. 6,000,006 to Bruce et al. ("Bruce").

Item 10 of the Office Action, as in the previous Office Action, suggests that lines 55-59 of column 2 of Bruce offer motivation for reconfiguring Assar to feature the invention as recited in claims 1 and 7. The passage states "While these flash memories systems are useful, a more effective flash memory system is desired . . ." The flash memories described above that passage, however, are different than that of Assar. Line 31, for example, states "Periodically clearing the erase counters is undesirable because there is no way to determine the total number of erase/write cycles to a given block . . . their erase counters are periodically cleared to zero regardless of usage." Assar, by contrast, does not clear the erase counters until all blocks have the identical amount of usage (page 20, line 36 to page 21, line 2).

In particular, Bruce describes at column 2, lines 24(25)- 30(31), that a prior art technique includes an erase counter which is incremented each time a respective portion of memory is erased and written. That is, in non-volatile memories such as EEPROMs and flash memories, each writing operation requires a preceding delete operation (present specification, page 1, lines 10-14). Returning to Bruce, in that prior art technique, once a portion of memory reaches a threshold erase count, it is moved to an

unused portion of memory. Once all unused pages are depleted, a clean-out erase cycle is performed. This periodic clearing of erase counters is undesirable (Bruce, col. 2, line 31: "undesirable"), because, due to the periodic across-the-board clearing and due to the movement to unused portions of memory, some portions of memory are subject to widely different usage from other portions of memory. As an example, constant erasing/re-writing of a single portion of memory would eventually exceed the count, and continued constant erasing/re-writing of that same portion of memory would flood out to fill all unused portions of memory thereby causing a memory-wide cleaning. Yet, the use count of that one portion varies widely from that of other portions. Due to the undesirability of widely uneven usage of portions of memory, Bruce resorts to retaining the total-write count for each portion of memory, and performs wear-leveling for a block when both the total and incremental counts for the block exceed respective thresholds.

As mentioned above, Assar differs in that Assar does not clear the erase counters until all blocks have the identical amount of usage (page 20, line 36 to page 21, line 2). Therefore, over time, the usage counts remain fairly uniform across the memory. This means that there is a lack of motivation for re-designing Assar in view of Bruce.

This is especially the case given the amount of overhead the proposed embodiment would take on. That is, Assar clears the erase inhibit flags concurrently with clearing the counters. What would have been the motivation for increasing the field size for the wearout leveling count and for the limit value? Not only is more storage required, but more resources are consumed in comparing the two quantities due to their larger size. Redesigning Assar to resemble the invention as recited in claim 1 would not have been obvious for at least the above-stated reasons.

The applicant further notes that even if motivation were deemed to exist, since Bruce increases a limit value only after a plurality of numbers exceed respective thresholds, Bruce fails to disclose or suggest, "increasing a limit value when a predetermined number . . . exceed the limit value" as explicitly required by the language of claims 1 and 7.

For at least all of the above reasons, Bruce fails to provide motivation to modify Assar to feature the limitations of the present invention as recited in claims 1 and 7, and claim 1 is not rendered obvious by the cited references.

Claim 15 depends from claim 1, and is not rendered obvious by the proposed combination of references at least for the same reasons. Support claim 15 as amended is found in the specification (e.g., page 7, lines 25-29: "To avoid the block 22 being erased many more times . . . selecting a block whose counter has a lower value . . ."; page 6, line 25: "computer system"). In other words, the data from that selected block, which is copied to "the first block (22)," may still be mutated (unlike in Assar), but probably will not be mutated "many more times" due to the lower-usage characteristic of the data.

Once again, the patentability of claim 15 is dismissed in a single sentence devoted also to claims 1, 7 and 13, but the patentable weight of the specific claim 15 limitations cannot fairly be ignored.

The rejection of claims 1-3, 5-9 and 11-13 and 16 based on Bruce cannot be maintained. Reconsideration and withdrawal of the rejection is respectfully requested.

Claim 14 stands rejected under 35 U.S.C. 103(a) as unpatentable over Assar in view of Bruce, or, alternatively, over Assar in view of Bruce and U.S. Patent No. 6,092,160 to Marsters.

Claim 14 depends from claim 1. Marsters is directed to block wear-leveling, but cannot make up for the deficiencies in Assar and Bruce. Accordingly, the proposed combination of references fails to render obvious the invention as recited in claim 14.

As to the remaining rejected claims, they each depend from one of the base claims and are likewise deemed to be obvious for at least the same reasons.

Notably, claim 17 stands rejected as indefinite but is not mentioned with respect to any of the rejections based on the prior art. This presumably would indicate that claim 17 is deemed to be allowable if its purported indefiniteness is overcome. Since the rejection for indefiniteness has been met, as set forth above, is apparently allowable even if any of the prior art rejections were to be deemed valid. Since, however, all of the prior art and other claim rejections have been shown above to be invalid, all of the rejected claims are allowable over the prior art applied.

Although item 20 of the Office Action suggests that "a flash memory system designer" is well aware of the Assar technique of zeroing out wear level counts and of the technique employed in the present invention and might choose one or the other method in view of the respective tradeoffs, item 20 falls short of demonstrating this purported proposition by finding prior art that discloses the method of the present invention. Instead, we are asked to imagine that it would have been obvious, and moreover, that it would have been "obvious" to re-configure Assar to feature the

inventive method of the present invention. The authority for such a proposition is apparently no more than the Examiner being taken with the idea of the present invention and concluding that someone out there must therefore have thought of it.

Apparently predicting the difficulty in proffering such a proposition, item 21 of the Office Action holds out the alternative suggestion that the proposed re-design of Assar would have been "obvious" in view of Bruce. As set forth above, this analysis too lacks merit.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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